# **Dual Differential Data and Clock D Flip-Flop With Set and Reset**

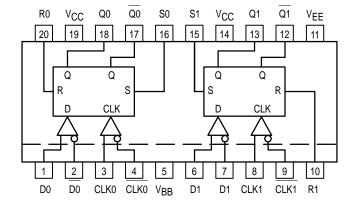
The MC100LVEL29 is a dual master–slave flip flop. The device features fully differential Data and Clock inputs as well as outputs. The MC100EL29 is pin and functionally equivalent to the MC100LVEL29 but is specified for operation at the standard 100E ECL voltage supply. A VBB output is provided for AC coupling, refer to the interfacing section of the ECLinPS Data Book (DL140) for more information on AC coupling ECL signals. Data enters the master latch when the clock is LOW and transfers to the slave upon a positive transition on the clock input.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to VEE and the D input will bias around VCC/2. The outputs will go to a defined state, however the state will be random based on how the flip flop powers up.

Both flip flops feature asynchronous, overriding Set and Reset inputs. Note that the Set and Reset inputs cannot both be HIGH simultaneously.

- 1100MHz Flip-Flop Toggle Frequency
- 20-lead SOIC Package
- 580ps Propagation Delays

#### Logic Diagram and Pinout: 20-Lead SOIC (Top View)



## MC100LVEL29 DC CHARACTERISTICS ( $V_{EE}$ = -3.0V to -3.8V; $V_{CC}$ = GND)

### MC100LVEL29 MC100EL29



#### **TRUTH TABLE**

R	S	D	CLK	Q	Ια
L H L	TITL	L H X X	Z Z X X	L H L H Undef	H L H L Undef

Z = LOW to HIGH Transition

#### **PIN NAMES**

Pins	Function
D0-D1	Data Inputs
R0-R1	Reset Inputs
CLK0-CLK1	Clock Inputs
S0-S1	Set Inputs

		-40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Unit									
IEE	Power Supply Current		35	50		35	50		35	50		35	50	mA
V <sub>BB</sub>	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
ΊΗ	Input HIGH Current			150			150			150			150	μΑ
IIL	Input LOW Current Dn Inputs Dn Inputs	0.5 -300			0.5 -300			0.5 -300			0.5 -300			μΑ

MC100LVEL29 AC CHARACTERISTICS ( $V_{EE} = -3.0V$  to -3.8V;  $V_{CC} = GND$ )

		–40°C				0°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit	
fMAX	Maximum Toggle Frequency	1.1			1.1			1.1			1.1			GHz	
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay CLK to Output S, R	480 480		680 700	490 490		690 710	500 500		700 720	520 520		720 740	ps	
ts tH	Setup Time Hold Time	0 100			0 100			0 100			0 100			ps	
<sup>t</sup> RR	Set/Reset Recovery	100			100			100			100			ps	
tpW	Minimum Pulse Width CLK, Set, Reset	400			400			400			400			ps	
VPP	Minimum Input Swing	150			150			150			150			mV	
V <sub>CMR</sub> 1	Common Vpp<500mV Mode RangeVpp≥500mV	-2.0 -1.8		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	V	
t <sub>r</sub>	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	280		550	ps	

The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within
the specified range and the peak-to-peak voltage lies between V<sub>PP</sub>min and 1V. The lower end of the CMR range varies 1:1 with V<sub>EE</sub>. The
numbers in the spec table assume a nominal V<sub>EE</sub> = -3.3V. Note for PECL operation, the V<sub>CMR</sub>(min) will be fixed at 3.3V – |V<sub>CMR</sub>(min)|.

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**DC CHARACTERISTICS** ( $V_{EE} = -4.2V \text{ to } -5.5V$ ;  $V_{CC} = GND$ )

		-40°C			0°C			25°C						
Symbol	Characteristic	Min	Тур	Max	Unit									
IEE	Power Supply Current		35	50		35	50		35	50		35	50	mA
V <sub>BB</sub>	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
ΙΗ	Input HIGH Current			150			150			150			150	μΑ
IIL	Input LOW Current Dn Inputs Dn Inputs	0.5 -300			0.5 -300			0.5 -300			0.5 -300			μА

#### MC100EL29

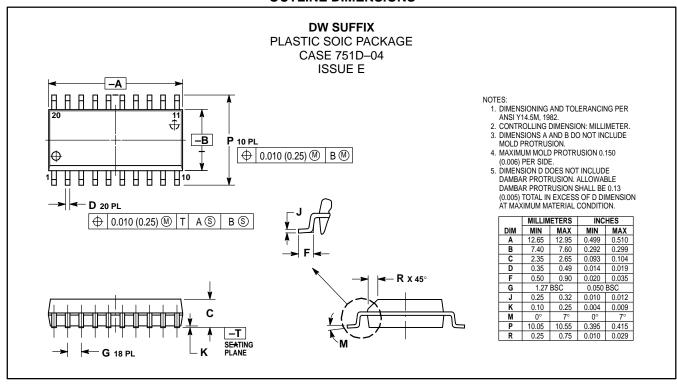
AC CHARACTERISTICS ( $V_{EE} = -4.2V$  to -5.5V;  $V_{CC} = GND$ )

		-40°C			0°C			25°C						
Symbol	Characteristic	Min	Тур	Max	Unit									
f <sub>MAX</sub>	Maximum Toggle Frequency	1.1			1.1			1.1			1.1			GHz
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay CLK to Output S, R	480 480		680 700	490 490		690 710	500 500		700 720	520 520		720 740	ps
ts t <sub>H</sub>	Setup Time Hold Time	0 100			0 100			0 100			0 100			ps
<sup>t</sup> RR	Set/Reset Recovery	100			100			100			100			ps
tpW	Minimum Pulse Width CLK, Set, Reset	400			400			400			400			ps
VPP	Minimum Input Swing	150			150			150			150			mV
V <sub>CMR</sub> 1	Common Vpp<500mV Mode RangeVpp≥500mV	-3.2 -3.0		-0.4 -0.4	-3.3 -3.1		-0.4 -0.4	-3.3 -3.1		-0.4 -0.4	-3.3 -3.1		-0.4 -0.4	V
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	280		550	ps

<sup>1.</sup> The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between Vppmin and 1V. The lower end of the CMR range varies 1:1 with VEE. The numbers in the spec table assume a nominal VEE = -4.5V. Note for PECL operation, the VCMR(min) will be fixed at 5.0V – |VCMR(min)|.

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